Course Type	Course Code	Name of Course	L	T	P	Credit
DC	NECC513	CAD for VLSI	3	1	0	4

Course Objective

With this course students will learn the fundamentals of Computer-Aided Design (CAD) tools for the modeling, design, analysis, test, and verification of digital VLSI systems. This is a demanding topic for industries working in VLSI domain.

Learning Outcomes

Upon successful completion of this course, students will:

- Acquire knowledge about CAD tools used for digital VLSI design, digital logic simulation and physical design, including test and verification.
- Model digital systems at different levels of abstraction.
- Simulate and verify a design.
- Transfer a design from a version possible to simulate to a version possible to synthesize.
- Develop understanding of FPGA CAD flow for design and implementation.

Module No.	Topics to be Covered	Lecture Hours	Learning Outcome
1	Basics of combinational and sequential logic circuits; Concept of delays in logic gates; Evolution of design automation; CMOS realizations of basic gates. Behavioral, structural and physical models, design flow, Types of CAD tools, introduction to logic simulation and synthesis.	9L+3T	Acquire an understanding of need and evolution of CAD tools for digital design flow.
2	Syntax, hierarchical modeling, HDL construct, simulator directives, instantiating modules, gate level modeling, Event based and level sensitive timing control, memory initialization, conditional compilation, time scales for simulation.	10L+4T	Learn about the basic syntax, hierarchical modeling style and event control using HDL.
3	Delay, switch level modeling, user defined primitive (UDP), memory modeling.	9L+2T	This unit helps the students to learn modeling of a digital hardware at transistor/switch level, modeling memory.
4	Logic synthesis of HDL construct, technology cell library, design constraints, Synthesis of HDL construct, Various optimization techniques, design size.	10	This unit helps the students to understand synthesis of a digital hardware, various constraints required and various optimization techniques useful for synthesis.
5	Commercial FPGA architecture, LUT and routing architecture, FPGA CAD flow, Typical case studies.	4	Learn about FPGA architecture, CAD flow for FPGA based design.
6	Introduction to Finite State Machines (FSM) and State Diagrams, Different Types of FSM, Modeling of FSM using HDL, Overview of Static Timing Analysis (STA), Setup and Hold Timing Analysis, Clock Skew and Jitter, Maximum clock frequency.	5	Learn about FSM and its representation using state diagram, Some real life examples of FSM like sequence detector, vending machine, traffic light controller This unit also helps the students to deal with different timing problems that arise during design of a digital system, avoid setup and hold violation, find maximum operating frequency of a digital system.
	Total	**56**	

Textbook:

1. S. H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons Publisher, 2nd Edition, 2008.
2. Z.Navabi, "Digital Design and Implementation with Field Programmable Devices", 1stEdition, Kluwer Academic Publishers, 2005.

Reference Books:

1. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", 2nd Edition, Pearson Publishers.
2. Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", McGraw Hill Publisher, 1994.
3. Naveed Shervani, "Algorithms for VLSI Physical Design Automation", Springer International Edition, 3rd Edition, 2005.
4. Wayne Wolf, "FPGA-BasedSystemDesign",PearsonPublisher,2004